AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A semiconductor memory device comprising:

a memory cell array formed by arranging memory cells in a matrix;

a plurality of word-lines for selecting each row of the memory cell array;

a plurality of bit-lines for carrying a data signal that is output by a memory cell belonging to each column of the memory cell array;

a reference signal generator part for generating a reference signal ~~that is to be a reference signal~~ when amplifying a data signal occurring on the bit-line; ~~and~~

an amplifier part for amplifying the data signal occurring on the bit-line ~~with~~ when comparing it with the reference signal~~;~~; and

~~characterized in that the semiconductor memory device has~~

a reference potential setup circuit part for setting up a potential assigned from outside of the device as a potential of the reference signal.

2. (currently amended): The semiconductor memory device according to claim 1, ~~characterized in that~~wherein the reference potential setup circuit part comprises:~~;~~

a transistor in which a drain terminal is connected to a bit-line in the memory cell array that is a line having the reference signal, ~~and~~ the potential assigned from outside of the device is provided to a source terminal, and a control signal activated in measurement of bit-line potential is provided to a gate terminal.

3. (currently amended): A testing system for testing a semiconductor memory device comprising a memory cell array formed by arranging memory cells in a matrix, a plurality of word-lines for selecting each row of the memory cell array, a plurality of bit-lines for carrying a data signal that is output by a memory cell belonging to each column of the memory cell array, a reference signal generator part for generating a reference signal ~~that is to be a reference signal~~ when amplifying the data signal occurring on the bit-line, an amplifier part for amplifying the data signal occurring on the bit-line ~~with~~ when comparing it with the reference signal, and a reference potential setup circuit part ~~for set up a potential assigned from outside of the device as potential of the reference signal, characterized in that the testing system comprises~~comprising:

a reference signal control part for generating a potential between a source potential and a ground potential ~~with~~ when varying the potential in one direction, ~~to apply~~applying it to the reference potential setup circuit, and controlling the potential of the reference signal;

a control part for controlling a series of steps ~~of~~ for generating an address ~~to provide it to~~for the semiconductor memory device and reading a data signal from the memory cell;

a determination part for determining a logic value of a data signal amplified by the amplifier part;

a storage part for storing a potential value of the reference signal when the logic value determined by the determination part is inverted; and

a statistical process part for statistically processing the value of the potential stored in the storage part;

wherein the reference potential setup circuit part for setting up a potential assigned from outside of the device as a potential of the reference signal.

4. (currently amended): The semiconductor memory device according to claim 1 ~~or 2, characterized in that~~ wherein the device comprises ~~all or some~~ at least one of the functions implemented by ~~the~~ a control part, a determination part, a storage part and a statistical process part ~~as set forth in claim 3.~~and wherein

said function of said reference signal control part is generating a potential between a source potential and a ground potential when varying the potential in one direction, applying it to the reference potential setup circuit, and controlling the potential of the reference signal;

said function of said reference potential setup circuit part is setting up a potential assigned from outside of the device as a potential of the reference signal;

said function of said control part is controlling a series of steps for generating an address for the semiconductor memory device and reading a data signal from the memory cell;

said function of said determination part is determining a logic value of a data signal amplified by the amplifier part;

said function of said storage part is storing a potential value of the reference signal when the logic value determined by the determination part is inverted; and

said function of said statistical process part is statistically processing the value of the potential stored in the storage part.

5. (currently amended): A testing method for testing a semiconductor memory device comprising a memory cell array formed by arranging memory cells in a matrix, a plurality of word-lines for selecting each row of the memory cell array, a plurality of bit-lines for carrying a data signal that is output by a memory cell belonging to each column of the memory cell array, a reference signal generator part for generating a reference signal ~~that is to be a reference signal~~ when amplifying a data signal occurring on the bit-line, an amplifier part for amplifying the data signal occurring on the bit-line ~~with~~ when comparing it with the reference signal, and a reference potential setup circuit part ~~for set up a potential assigned from outside of the device as potential of the reference signal, characterized in that the method comprises the steps of~~comprising:

(a) setting up a potential assigned from outside of the device as potential of the reference signal;~~setting up potential of the reference signal by the reference potential setup circuit part;~~

(b) reading out a data signal from the memory cell to the bit-line; and

(c) comparing for magnitude relationship in potential, the reference signal and data signal compared by the amplifying part to obtain the potential of the reference signal when the magnitude relationship inverts.

6. (currently amended): A semiconductor memory device comprising:

_____ a memory cell array formed by arranging memory cells in a matrix~~,~~;

_____ a plurality of word-lines for selecting each row of the memory cell array~~,~~;

_____ a plurality of bit-lines for carrying data signal that is output by a memory cell belonging to each column of the memory cell array, and

_____an amplifier part for amplifying the data signal occurring on the bit-line, and

a signal hold circuit for taking and holding data signal read out to the bit-line.

7. (currently amended): The semiconductor memory device according to claim 6, ~~characterized~~ wherein ~~in that~~ the signal hold circuit comprises a sample hold circuit.

8. (currently amended): A testing system for testing a semiconductor memory device comprising a memory cell array formed by arranging memory cells in a matrix, a plurality of word-lines for selecting each row of the memory cell array, a plurality of bit-lines for carrying data signal that is output by a memory cell belonging to each column of the memory cell array, an amplifier part for amplifying the data signal occurring on the bit-line, and a signal hold circuit for taking and holding a signal on the bit-line, ~~characterized in that the system comprises~~comprising:

a first control part for controlling a series of steps ~~of~~ for generating an address to provide it to the semiconductor memory device and reading out a data signal from the memory cell;

a second control part for controlling such that the signal hold circuit takes data signal read out to the bit-line;

a conversion part for A/D converting the data signal taken to the signal hold circuit;

a storage part for storing data signal A/D converted by the data conversion part; and

a statistical process part for statistically processing data stored in the storage part.

9. (currently amended): The semiconductor memory device according to claim 6 ~~or 7, characterized in that~~wherein the device comprises ~~all or some~~at least one of the functions implemented by ~~the~~ a first and second control parts, a conversion part, a storage part, and a

statistical process part ~~set forth in claim 8.~~and wherein

said function of said first control part is controlling a series of steps for generating an address to provide it to the semiconductor memory device and reading out a data signal from the memory cell;

said function of said second control part is controlling such that the signal hold circuit takes data signal read out to the bit-line;

said function of said conversion part is for A/D converting the data signal taken to the signal hold circuit;

said function of said storage part is storing data signal A/D converted by the data conversion part; and

said function of said statistical process part is statistically processing data stored in the storage part.

10. (currently amended): A testing ~~system~~ method for testing a semiconductor memory device comprising a memory cell array formed by arranging memory cells in a matrix, a plurality of word-lines for selecting each row of the memory cell array, a plurality of bit-lines for carrying a data signal that is output by a memory cell belonging to each column of the memory cell array, an amplifier part for amplifying the data signal occurring on the bit-line, and a signal hold circuit for taking and holding signal on the bit-line, ~~characterized in that the system comprises the steps of:~~ comprising:

(a) reading out a data signal from the memory cell to the bit-line;

(b) taking the data signal read out to the bit-line, to the signal hold circuit; and

(c) reading out the potential of data signal taken to the signal hold circuit, to outside.

11. (new): The semiconductor memory device according to claim 2, wherein the device comprises at least one of the functions implemented by a control part, a determination part, a storage part and a statistical process part and wherein

said function of said reference signal control part is generating a potential between a source potential and a ground potential when varying the potential in one direction, applying it to the reference potential setup circuit, and controlling the potential of the reference signal;

said function of said reference potential setup circuit part is setting up a potential assigned from outside of the device as a potential of the reference signal;

said function of said control part is controlling a series of steps for generating an address for the semiconductor memory device and reading a data signal from the memory cell;

said function of said determination part is determining a logic value of a data signal amplified by the amplifier part;

said function of said storage part is storing a potential value of the reference signal when the logic value determined by the determination part is inverted; and

said function of said statistical process part is statistically processing the value of the potential stored in the storage part.

12. (new): The semiconductor memory device according to claim 7, wherein the device comprises at least one of the functions implemented by a first and second control parts, a conversion part, a storage part, and a statistical process part and wherein:

said function of said first control part is controlling a series of steps for generating an address to provide it to the semiconductor memory device and reading out a data signal from the memory cell;

said function of said second control part is controlling such that the signal hold circuit takes data signal read out to the bit-line;

said function of said conversion part is for A/D converting the data signal taken to the signal hold circuit;

said function of said storage part is storing data signal A/D converted by the data conversion part; and

said function of said statistical process part is statistically processing data stored in the storage part.

13. (new): The semiconductor memory device according to claim 7, wherein said sample hold circuit comprises a capacitor and a voltage follower, a potential on the bit-line being selectively input to the voltage follower, the capacitor being arranged to maintain the selectively input potential of the bit line as input to the voltage follower, wherein a capacitance of said capacitor is lower than a parasitic capacitance of the bit-line.